AMENDMENTS

In the Claims

1. (Currently Amended) A method for analyzing input output (I/O) pin arrangements to determine the effect of differential pair and power and ground pin placement on signal quality comprising:

constructing an array of pins;

arranging a plurality of differential pairs within the array of pins to provide a pin arrangement;

exciting each of the differential pairs within the pin arrangement;

monitoring coupled noise on other differential pairs within the pin arrangement;

analyzing the pin arrangement based upon the monitoring, the analyzing the pin arrangement including

generating a coupling plot based upon the monitoring; and

determining cumulative coupling based upon the coupling plot.

2. (Cancelled)

3. (Original) The method of claim 1 wherein the pin arrangement includes: maximally packed differential pairs.

4. (Original) The method of claim 1 wherein the pin arrangement includes: power and ground pins as well as differential pairs.

5. (Original) The method of claim 4 wherein:

the differential pairs, power pins and ground pins are arranged according to a ratio of eight differential pairs per one power pin and one ground pin.

6. (Original) The method of claim 4 wherein the pin arrangement includes:

the differential pairs, power pins and ground pins are arranged according to a ratio of six different pairs per one power pin and one ground pin.

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7. (Original) The method of claim 4 wherein the pin arrangement includes:
the differential pairs, power pins and ground pins are arranged according to a ratio of four differential pairs per one power pin and one ground pin.

8. (Currently Amended) An apparatus for analyzing input output (I/O) pin arrangements to determine the effect of differential pair and power and ground pin placement on signal quality comprising:
means for constructing an array of pins;
means for arranging a plurality of differential pairs within the array of pins to provide a pin arrangement;
means for exciting each of the differential pairs within the pin arrangement;
means for monitoring coupled noise on other differential pairs within the pin arrangement;
means for analyzing the pin arrangement based upon the monitoring, the means for analyzing the pin arrangement including
means for generating a coupling plot based upon the monitoring; and
means for determining cumulative coupling based upon the coupling plot.

9. (Cancelled)

10. (Original) The apparatus of claim 8 wherein the pin arrangement includes:
maximally packed differential pairs.

11. (Original) The apparatus of claim 8 wherein the pin arrangement includes:
power and ground pins as well as differential pairs.

12. (Original) The apparatus of claim 11 wherein:
the differential pairs, power pins and ground pins are arranged according to a ratio of eight differential pairs per one power pin and one ground pin.

13. (Original) The apparatus of claim 11 wherein the pin arrangement includes:

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the differential pairs, power pins and ground pins are arranged according to a ratio of six different pairs per one power pin and one ground pin.

14. (Original) The apparatus of claim 11 wherein the pin arrangement includes:
the differential pairs, power pins and ground pins are arranged according to a ratio of four differential pairs per one power pin and one ground pin.

15. (Currently Amended) An apparatus comprising:
a processor;
a memory coupled to the processor; and
a system for analyzing input output (I/O) pin arrangements to determine the effect of differential pair and power and ground pin placement on signal quality, the system being stored on the memory and executing on the processor, the system including
a constructing module, the constructing module constructing an array of pins;
an arranging module, the arranging module arranging a plurality of differential pairs within the array of pins to provide a pin arrangement;
an exciting module, the exciting module exciting each of the differential pairs within the pin arrangement;
a monitoring module, the monitoring module monitoring coupled noise on other differential pairs within the pin arrangement; and,
an analyzing module, the analyzing module analyzing the pin arrangement based upon the monitoring the analyzing module including
a generating module, the generating module generating a coupling plot based upon the monitoring; and
a determining module, the determining module determining cumulative coupling based upon the coupling plot.

16. (Cancelled)

17. (Original) The apparatus of claim 15 wherein the pin arrangement includes:
maximally packed differential pairs.

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18. (Original) The apparatus of claim 15 wherein the pin arrangement includes: power and ground pins as well as differential pairs.

19. (Original) The apparatus of claim 18 wherein:
the differential pairs, power pins and ground pins are arranged according to a ratio of eight differential pairs per one power pin and one ground pin.

20. (Original) The apparatus of claim 18 wherein the pin arrangement includes:
the differential pairs, power pins and ground pins are arranged according to a ratio of six different pairs per one power pin and one ground pin.

21. (Original) The apparatus of claim 18 wherein the pin arrangement includes:
the differential pairs, power pins and ground pins are arranged according to a ratio of four differential pairs per one power pin and one ground pin.

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